## REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner indicating that claims 19 and 23-27 are allowable and that claim 3 contains allowable subject matter.

**Disposition of Claims**

Claims 1, 3-19, and 23-27 are pending in this application. Claims 1, 18, and 19 are independent. The remaining claims depend, directly or indirectly, from claims 1 and 19.

In the response to the Office Action dated December 5, 2002, non-elected claims 7-17 were withdrawn from consideration. These claims are now canceled in this reply without prejudice or disclaimer.

Further, in this reply, claims 1, 3, 4, and 18 have been amended to clarify the present invention. Support for these amendments may be found in the specification, *e.g.*, Figures 3-4 and the accompanying description. Accordingly, no new matter has been added.

**Rejection(s) under 35 U.S.C § 112**

Claim 4 stands rejected under 35 U.S.C. § 112 as being indefinite. Claims 3 and 4 have been amended in view of the Examiner's comments. Thus, the rejection is now moot. Accordingly, withdrawal of the rejection is respectfully requested.

**Rejections Under 35 U.S.C. § 102**

Claims 1, 4-6, and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,969,576 ("Trodden"). Claims 1, 4, and 18 have been amended to clarify the present invention recited. To the extent that the rejection still applies to the remaining claims, the rejection is respectfully traversed.

As amended, independent claim 1 recites a computer system that comprises a phase locked loop and a lock detect indicator. The phase locked loop includes a phase-frequency detector that inputs a system clock and generates a chip clock, where the phase-frequency detector generates pulses on a first signal and a second signal dependent on a relationship between the system clock and the chip clock. Further, using the first and second signals, the lock

detect indicator determines whether the phase locked loop is out of lock dependent on whether a pulse on the first signal or the second signal is longer than a predetermined pulse width.

Similarly, as amended, independent claim 18 recites an integrated circuit that comprises generating means, detecting means, and indicating means. The generating means uses a first signal and a second signal to maintain a relationship between the chip clock and the system clock, the detecting means uses the first and second signals to determine whether the generating means is out of lock, and the indicating means indicates whether the generating means is out of lock dependent on whether a pulse on the first signal or the second signal is longer than a predetermined pulse width.

In the present application, Figure 3 shows that an embodiment of the present invention includes a lock detect indicator **42** and a phase locked loop **40**. The phase locked loop **40** includes a phase frequency detector **44** that inputs a system clock (**sys_clock**) and generates a chip clock (**chip_clk**). In addition, the phase-frequency detector **44** generates pulses on a first signal (**fast_pulse**) and a second signal (**slow_pulse**) dependent on a relationship between the system clock (**sys_clock**) and the chip clock (**chip_clk**). The lock detect indicator **42** uses the first and second signals (**fast_pulse** and **slow_pulse**) to determine whether the phase locked loop **40** is out of lock. Further, the lock detect indicator **42** determines whether the phase locked loop **40** is out of lock dependent on whether a pulse on the first signal (**fast_pulse**) or the second signal (**slow_pulse**) is longer than a predetermined pulse width. As shown in Figure 4, this determination is made in a first stage **50** of the lock detect indicator **42** by determining whether a width of the pulse is longer than a delay provided by a delay element **60**.

As acknowledged by the Examiner, Trodden does <u>not</u> teach that a lock detect indicator **100** includes circuitry for generating a first lock indication pulse dependent on whether a pulse on the first signal or the second signal is longer than a predetermined pulse width as recited in claim 3 of the present application. Claim 1 of the present application has been amended to include the limitation that the lock detect indicator uses the first and second signals to determine whether the phase locked loop is out of lock *dependent on whether a pulse on the first signal or the second signal is longer than a predetermined pulse width.* Further, claim 18 has been amended to include the limitation that the indicating means indicates whether the generating means is out of lock *dependent on whether a pulse on the first signal or the second signal is*

*longer than a predetermined pulse width*. In contrast with the amended claims, Trodden does not teach or suggest that his lock detect indicator **100** may be used for or has any need for measuring whether a pulse on the first signal or the second signal is longer than a predetermined pulse width in order to determine a lock status of the phase locked loop.

In view of the above, Trodden fails to show or suggest the present invention as recited in amended independent claims 1 and 18. Thus, the claims as amended are patentable over Trodden. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

**Conclusion**

Applicant believes this reply to be fully responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.139001).

Respectfully submitted,

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